Clock Tree Synthesis

How to Synchronize your own chip

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Design Status, Start of CTS Phase

- Placement - completed
- Power and ground nets – prerouted
- Estimated congestion - acceptable
- Estimated timing - acceptable (0ns slack)
- Estimated max cap/transition – no violations
- High fanout nets:
  1. Reset, Scan Enable synthesized with buffers
  2. Clocks are still not buffered

Design Status, Start of CTS Phase

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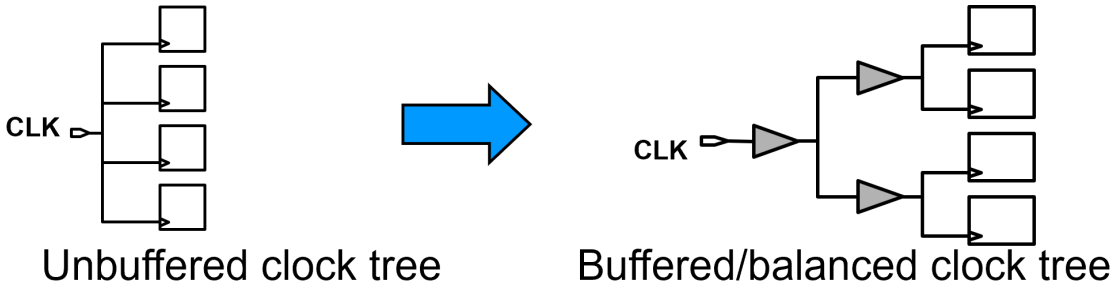
Question

Why are there no buffers on clock nets?

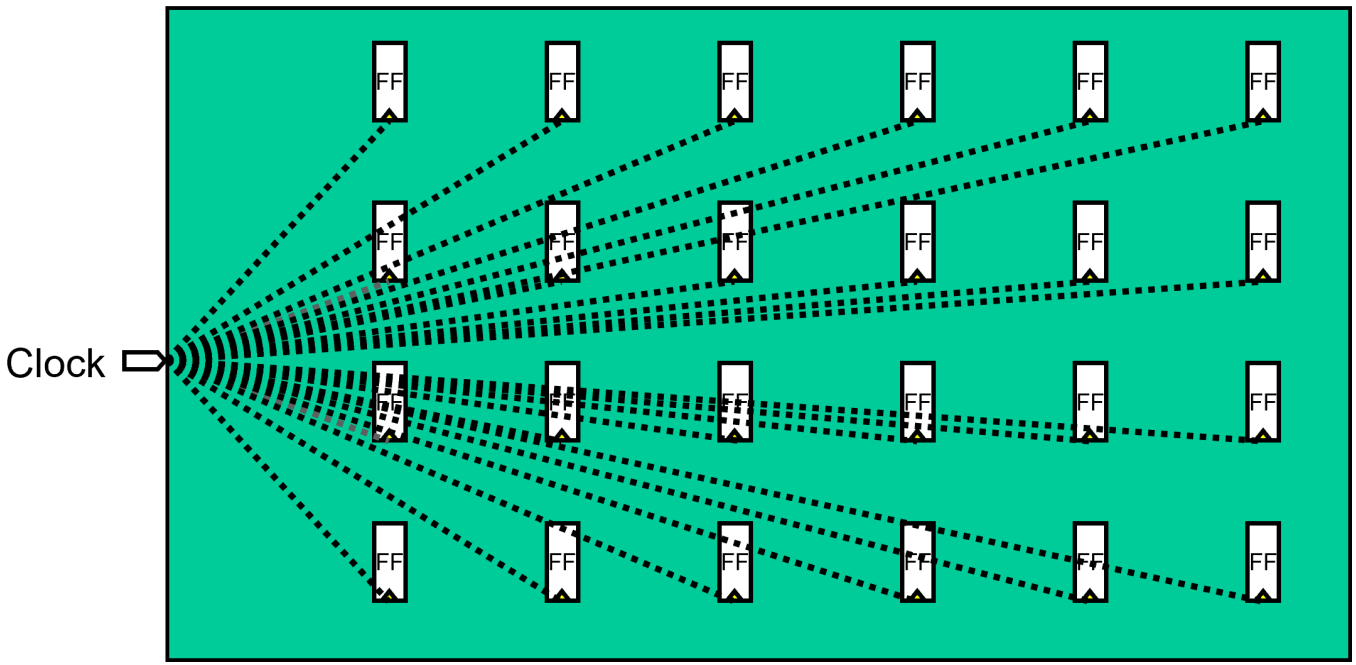
CTS Problem

- CTS is the process of distributing clock signals to clock pins based on physical/layout information
- After placement of cells the tree of synchronization is synthesized
- Balanced clock tree is synchronized with the addition of buffers
- After routing CT optimization is made



Starting Point before CTS

- All clock pins are driven by a single clock source
- All clock pins are from a source of clock pulses in various geometrical distances



CTS Goals

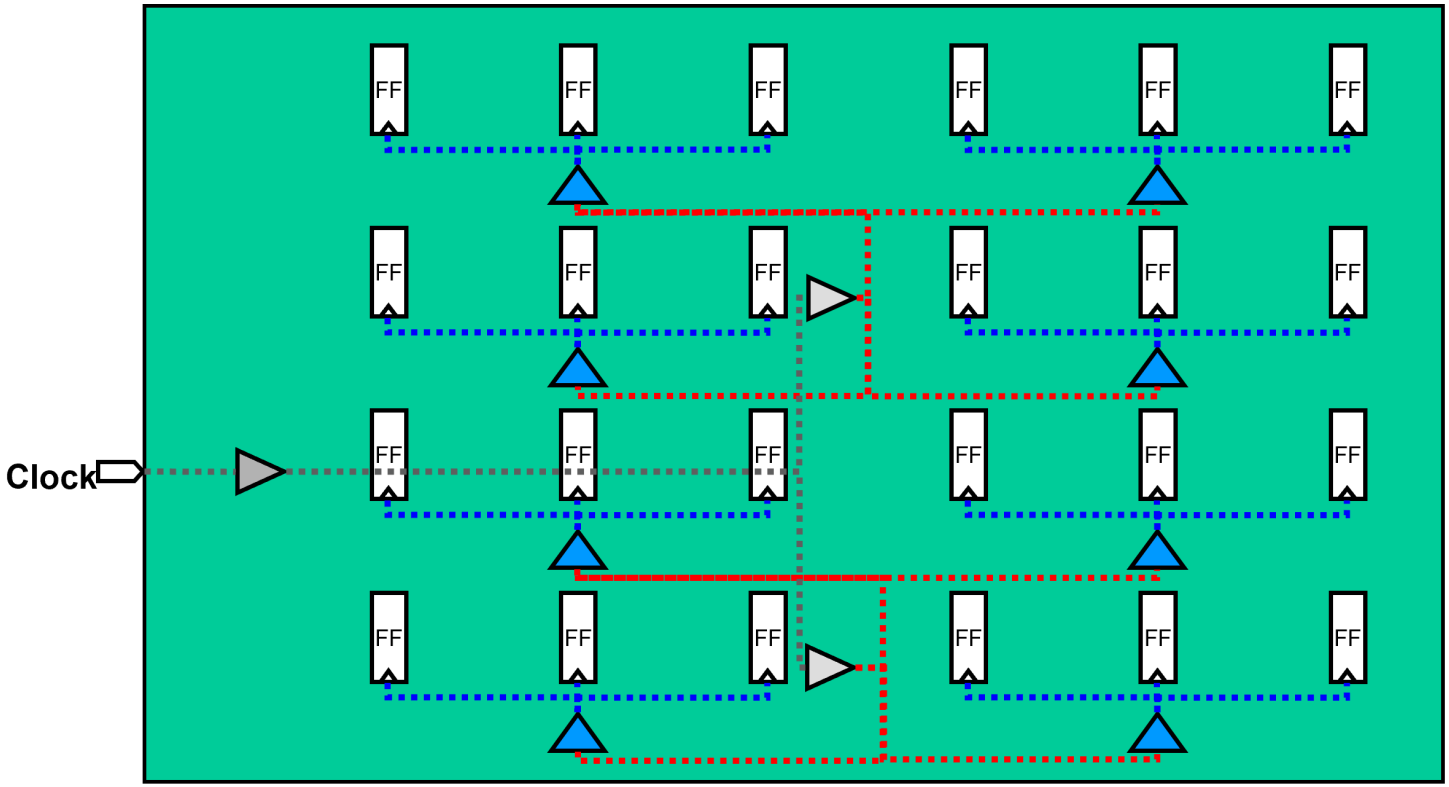
- **Meet the clock tree Design Rule Constraints (DRC):**
  - Maximum transition delay
  - Maximum load capacitance
  - Maximum fanout
  - Maximum buffer levels

Constraints are upper bound goals. If constraints are not met, violations will be reported.

- **Meet the clock tree targets:**
  - Maximum skew
  - Min/Max insertion delay

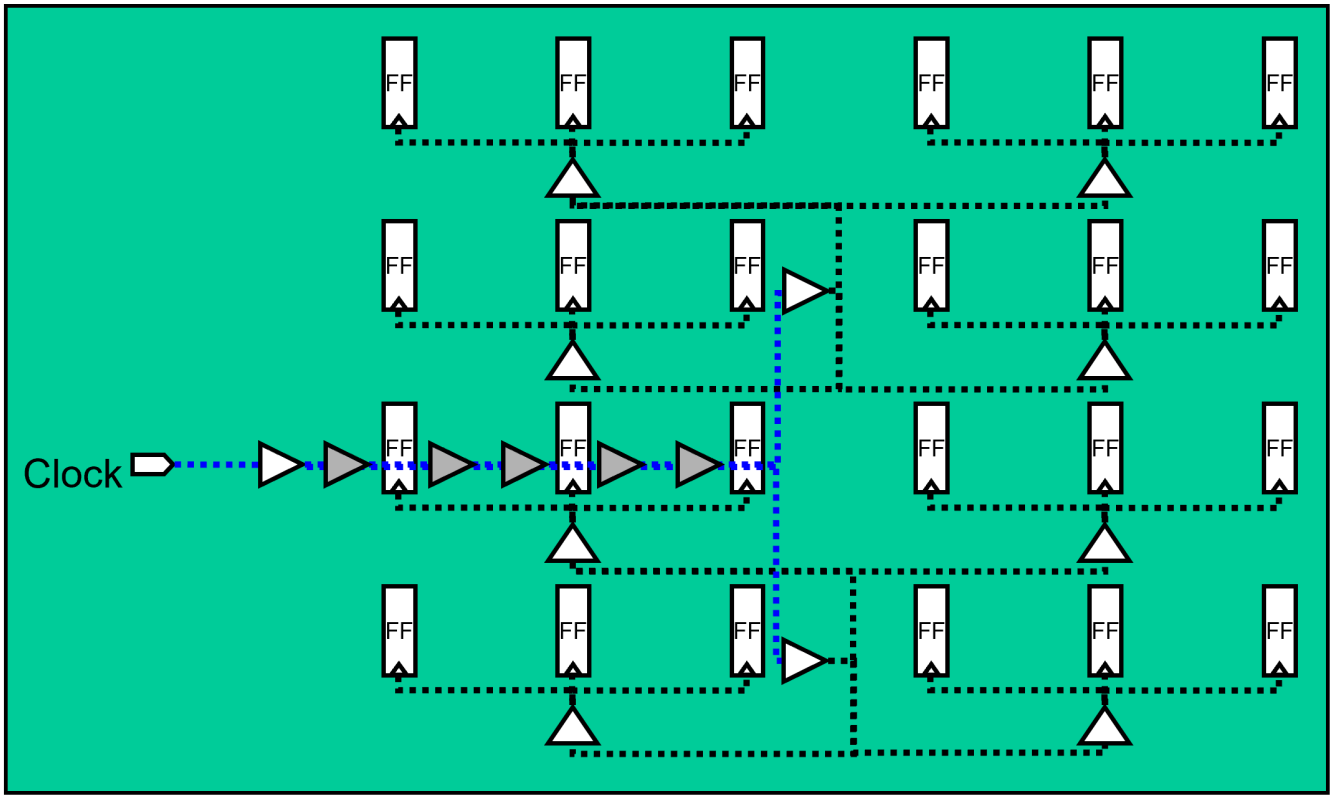
Targets are "nice to have" goals. If targets are not met, no violations will be reported.

Clock Tree Synthesis (CTS) (1/2)



A buffer tree is built to balance the loads and minimize the skew

Clock Tree Synthesis (CTS) (2/2)



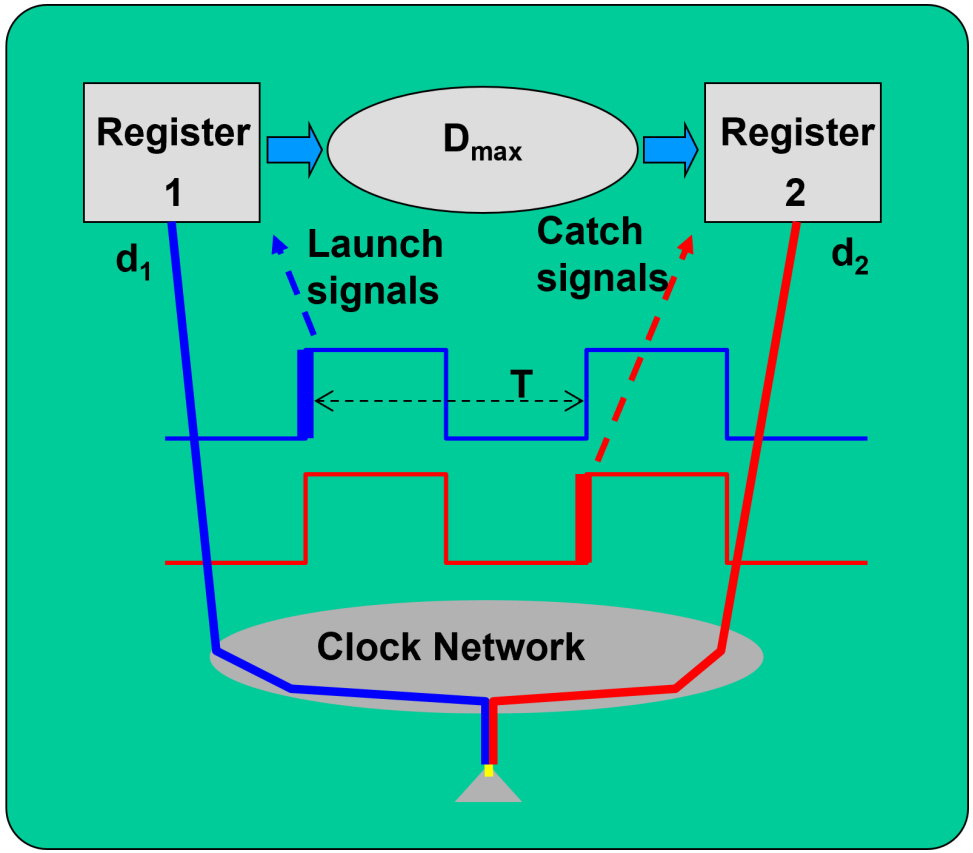
A delay line is added to meet the minimum insertion delay

Clock Tree: General Concepts: Clock Distribution Network

Skew = $d_1 - d_2$

Zero skew: $d_1 = d_2$

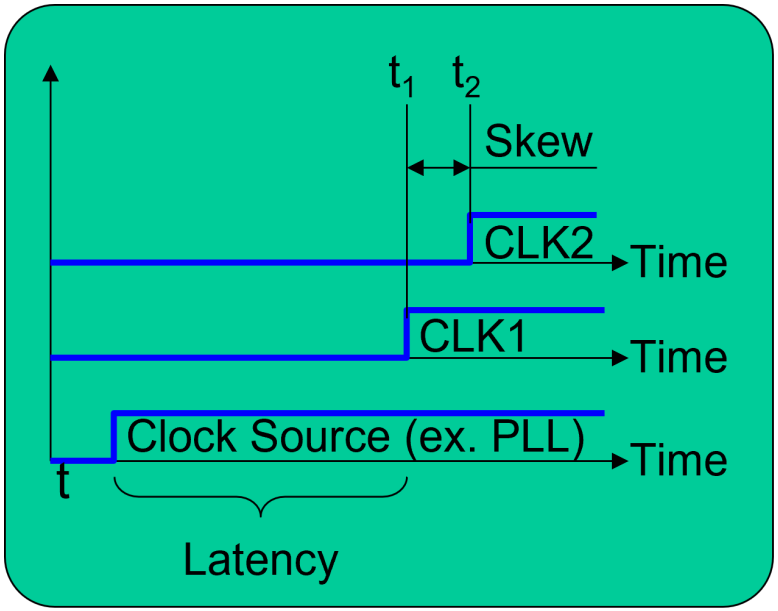
Useful skew, $d_1 - d_2 = \delta_{12}$

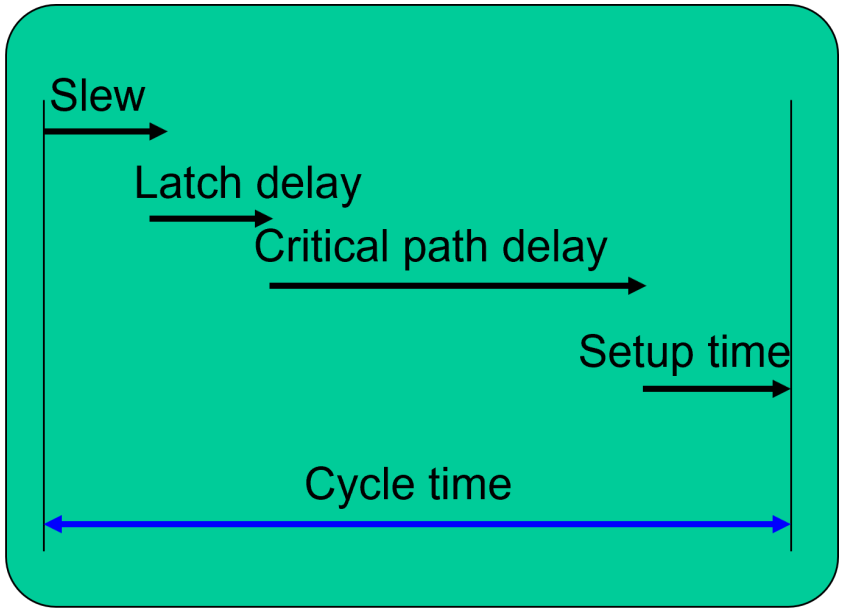


Clock Tree: General Concepts: Clock Tree Goal and Metrics

- **Goal**
  - Basic connectivity
- **Metrics**
  - Skew
  - Power
  - Area
  - Slew rates

Clock Tree: General Concepts: Clock Skew: Definition, Causes and Effects

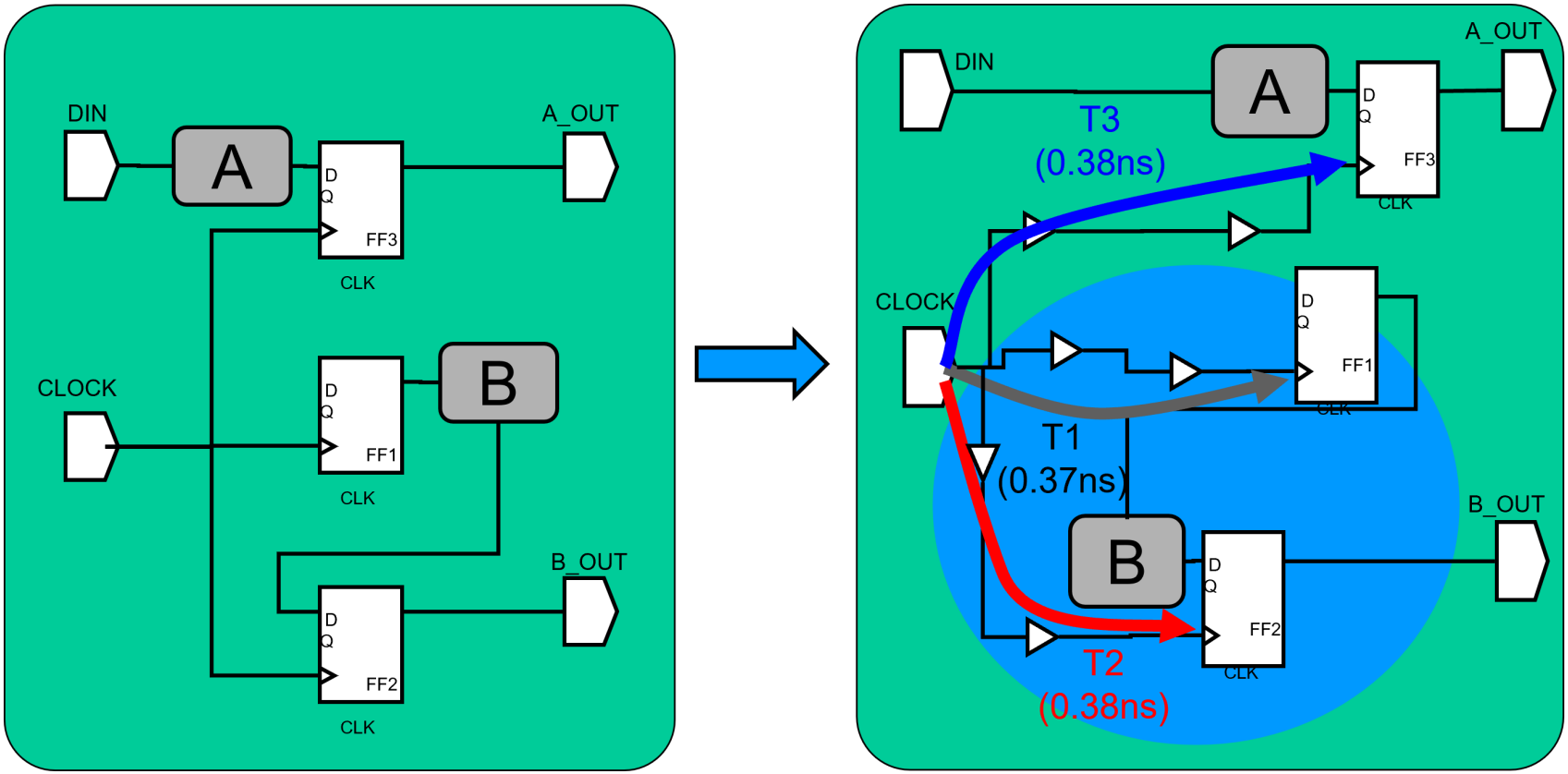




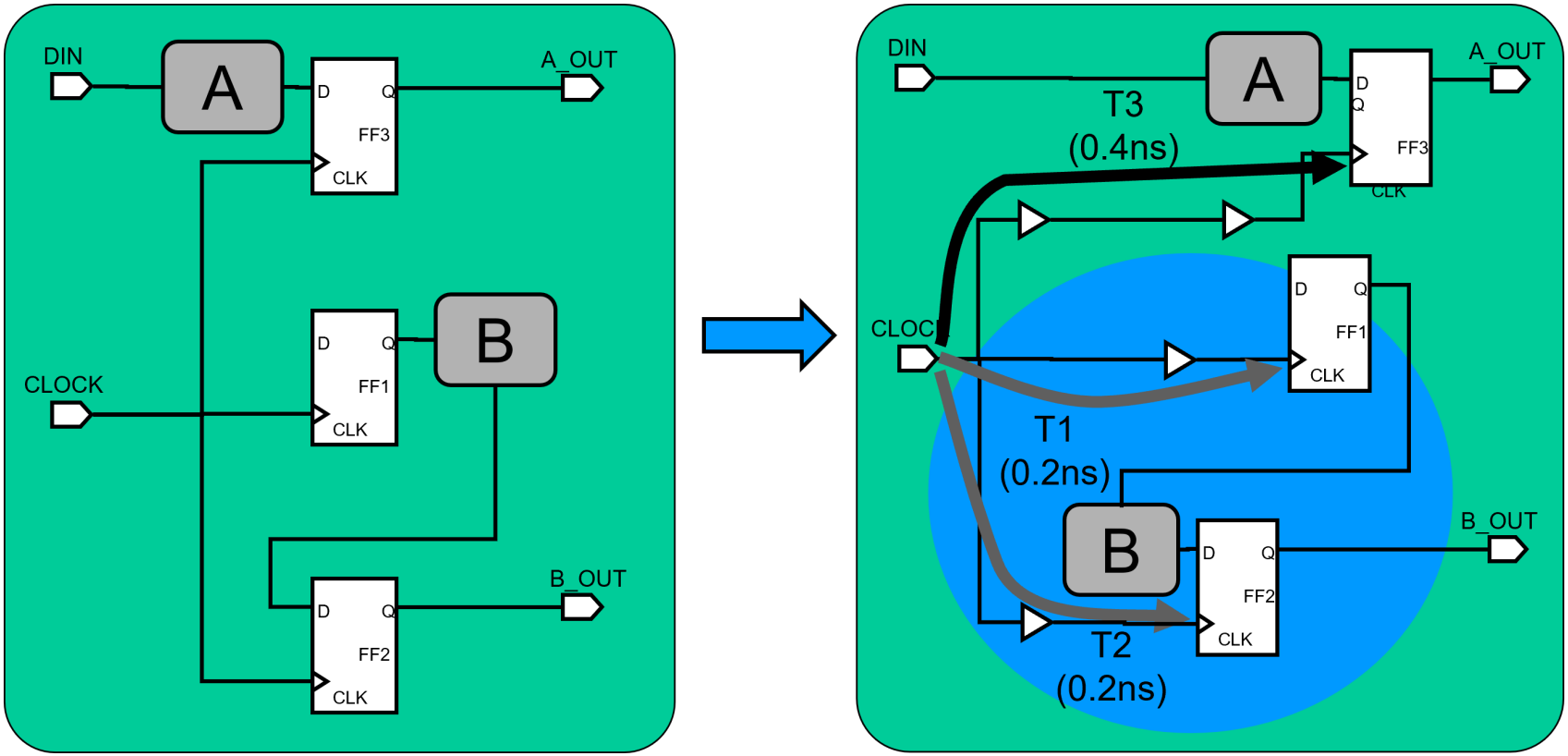
Clock Skew Types

- **Global**
  - Global skew is recommended - fastest
  - may add unnecessary buffers
- **Local**
  - Longer runtime
  - Possibly fewer buffers ” Only related FFs are balanced for skew ”
- **Useful**
  - Used to fix small violations where local or global failed

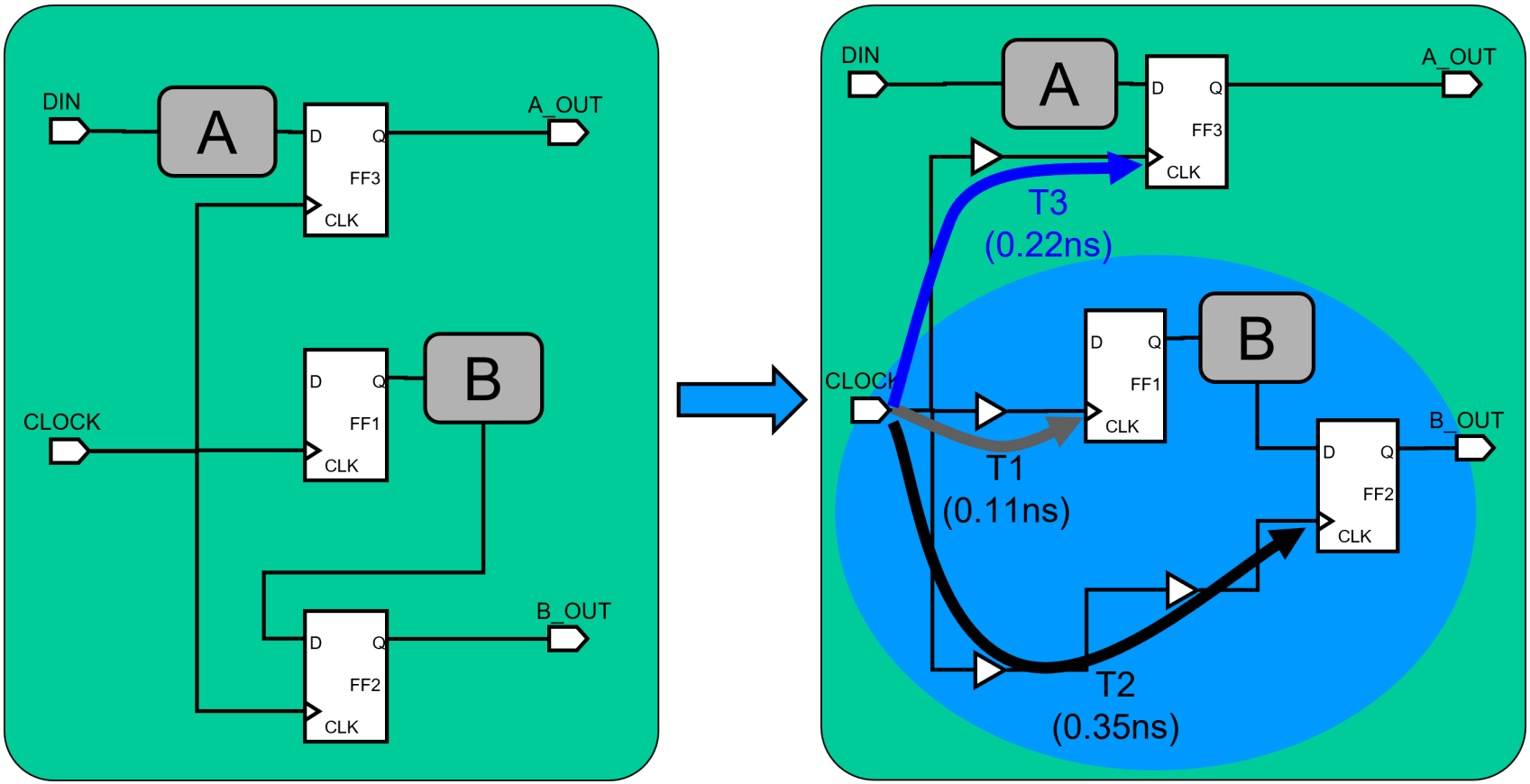
Global Skew: Fastest Runtime



Local Skew: Targeted Synthesis, But Slower



Useful Skew


DIN
A
A_OUT
D
Q
FF3
CLK
CLOCK
B
FF1
B_OUT
FF2
T3
(0.22ns)
T1
(0.11ns)
T2
(0.35ns)

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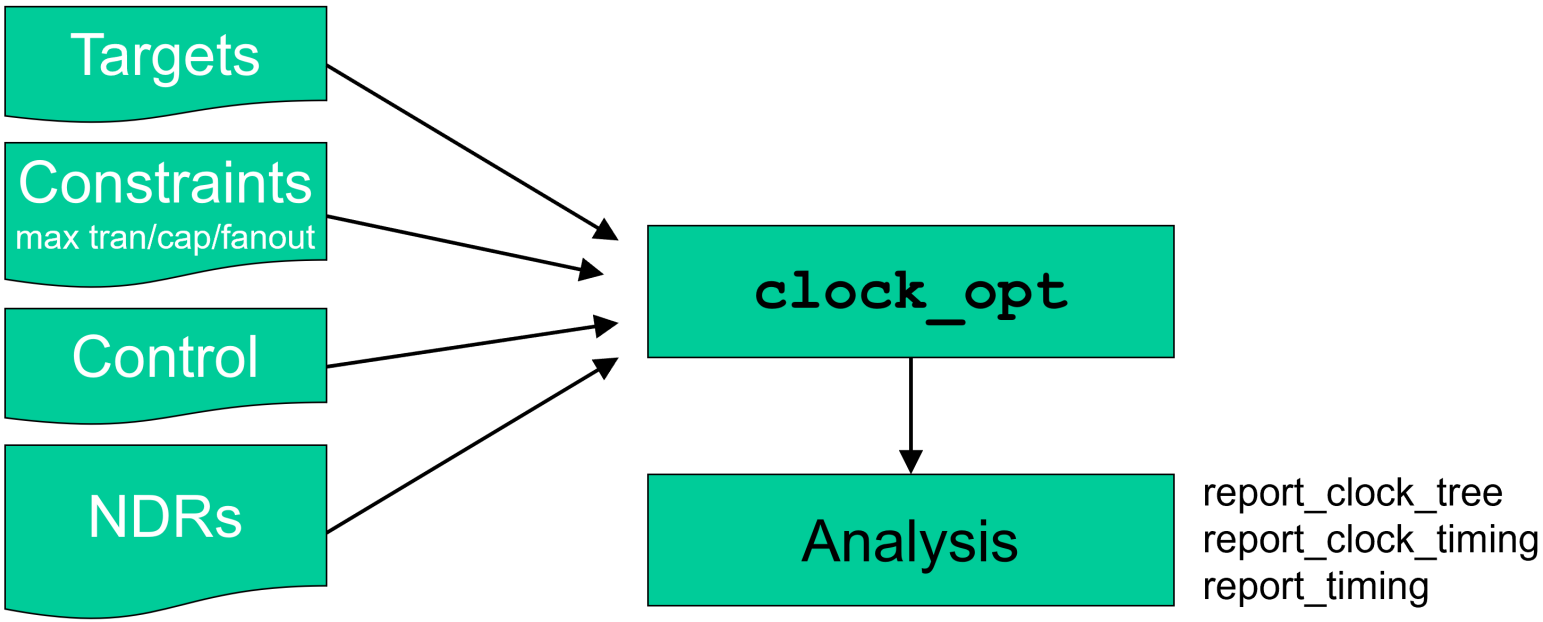
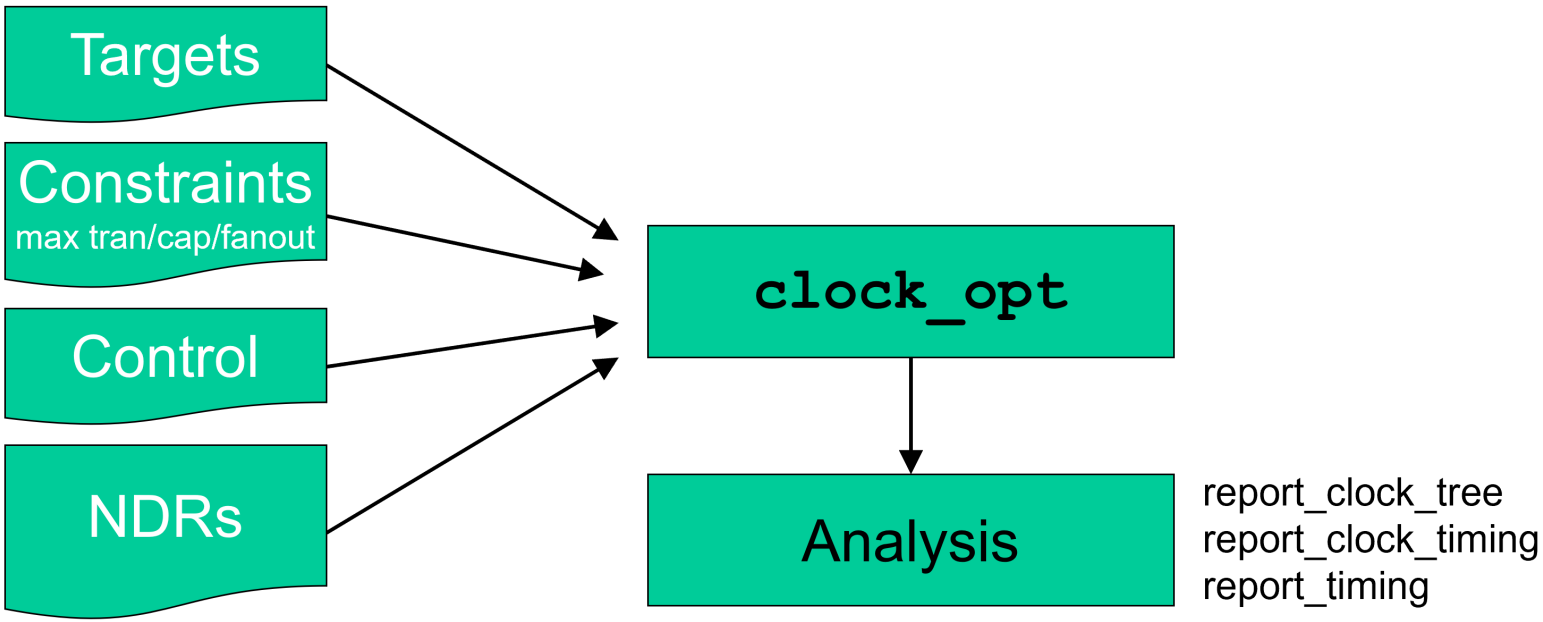
Clock Tree Synthesis



Clock Tree Synthesis



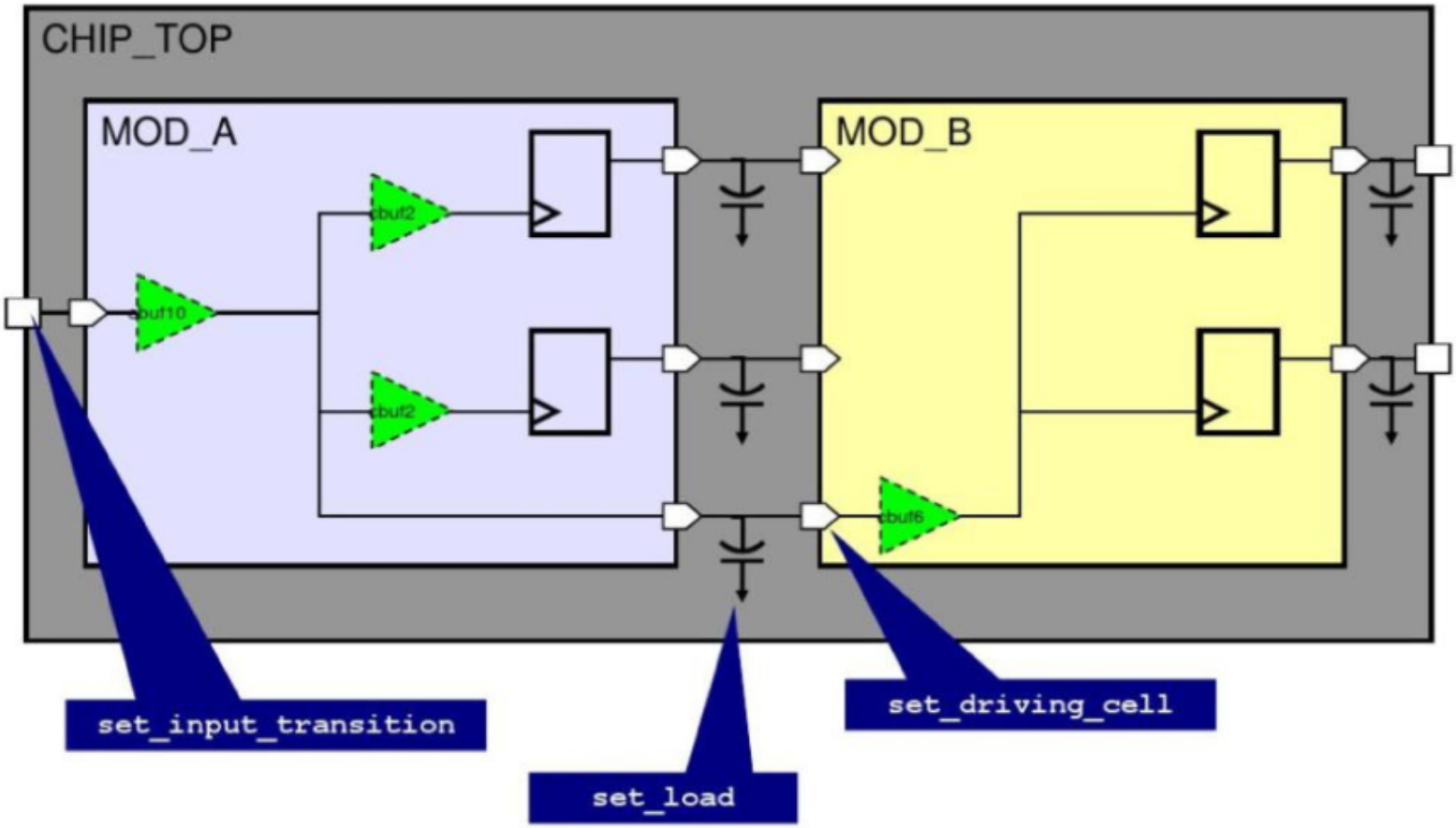
Understand Your Clock Tree Goals

- **Skew Goal**
  - What are the skew requirements for your design?
  - Are there different skew targets for small and large clocks?
- **Insertion Delay Goal**
  - What are the insertion delay specs for your block?
  - What is a reasonable target based on the size and floorplan of your block/chip?
- **Nondefault rules to prevent SI problems**
- **DRC Requirements**
  - Are signal net DRCs different from clock net DRCs?
- **Find out the order of significance or importance of all the clocks in the design**

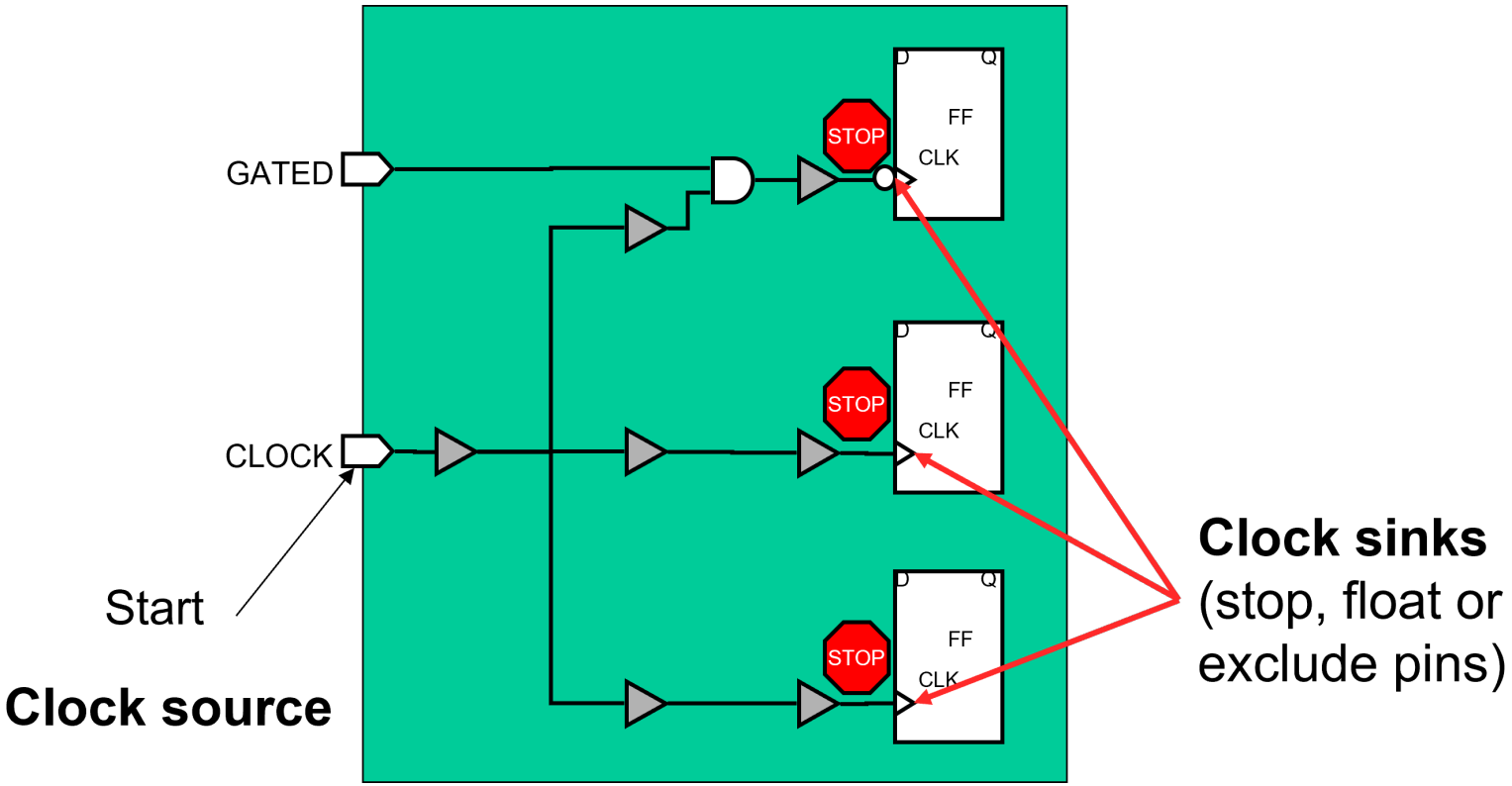
Default Clock Tree Targets

- **The default CTS target for skew and insertion delay is Ons**
  - Uncertainty and insertion delay SDC constraints are ignored
- **It is recommended to relax the clock skew target as much as possible**
  - Reduces overall buffer count, Power, and run time
- **Specify minimum clock latencies as needed**

Constraints: Are all Clock Drivers and Loads Specified?

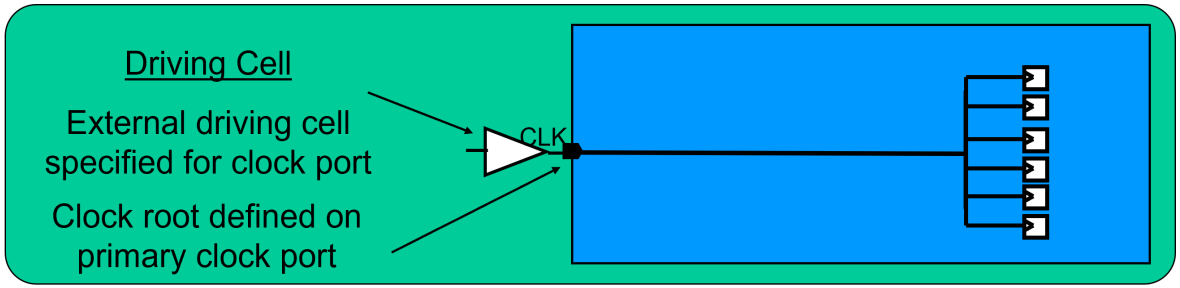


Where Does the Clock Tree Begin and End?



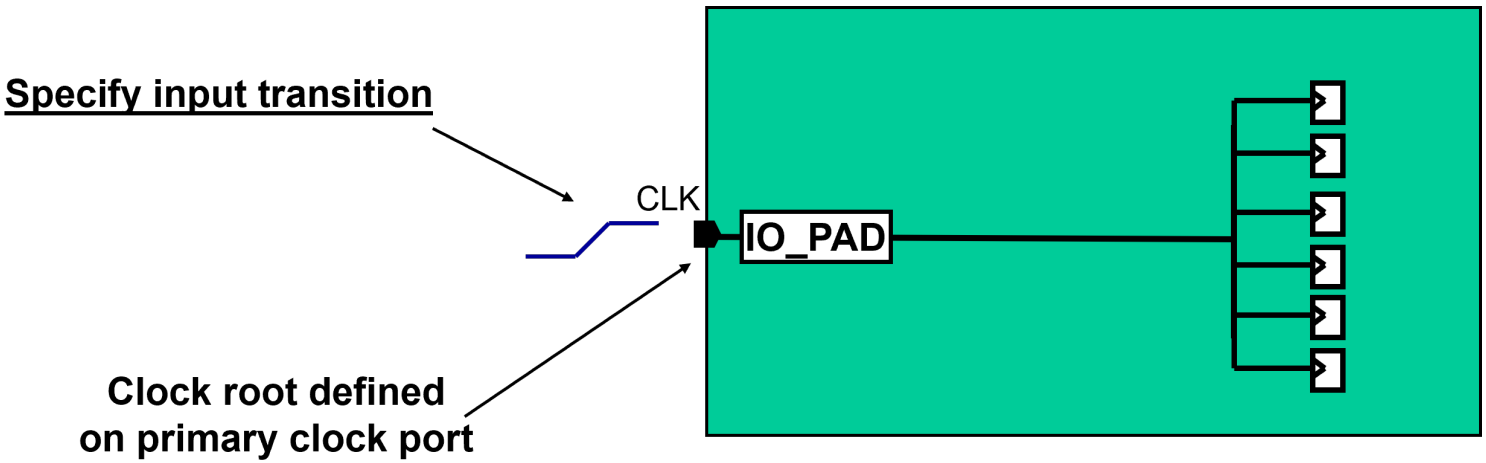
Define Clock Root Attributes (1/2)

- **When the clock root is a primary port of a block**
  - Ensure that an appropriate driving cell is defined
    set_driving_cell
  - The synthesis constraints may include a weak driving cell for all inputs, including the clock port
  - Because the clock is ideal during synthesis it has no effect on design QoR
  - But a weak driver on the clock port affects clock tree QoR during CTS



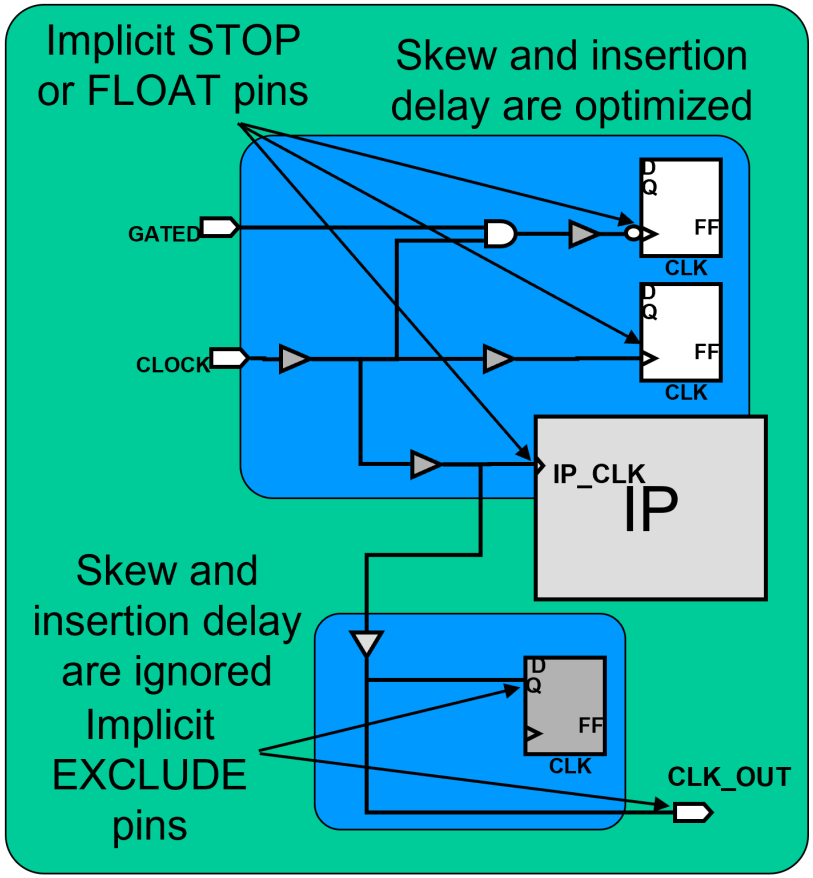
Define Clock Root Attributes (2/2)

- **When the clock root is a primary port, but at the CHIP-level through an IO-PAD**
  - Ensure that an appropriate input transition is defined
    set_input_transition

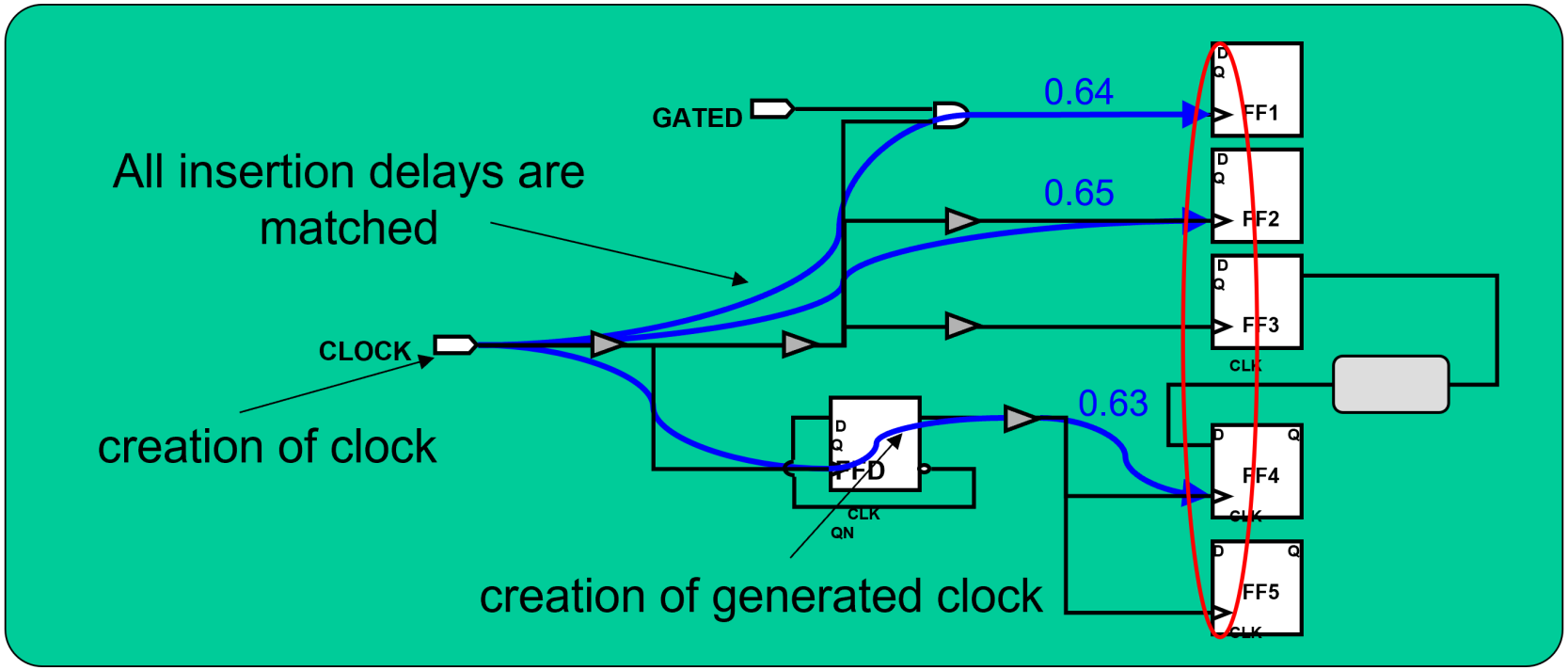


Stop, Float and Exclude Pins

- **Stop Pins:**
  - CTS optimizes for DRC and clock tree targets (skew, insertion delay)
- **Float Pins:**
  - Like Stop pins, but with delays on clock pin
- **Exclude (Ignore) Pins:**
  - CTS ignores skew and insertion delay targets
  - CTS will fix DRCs to meet library or SDC constraints



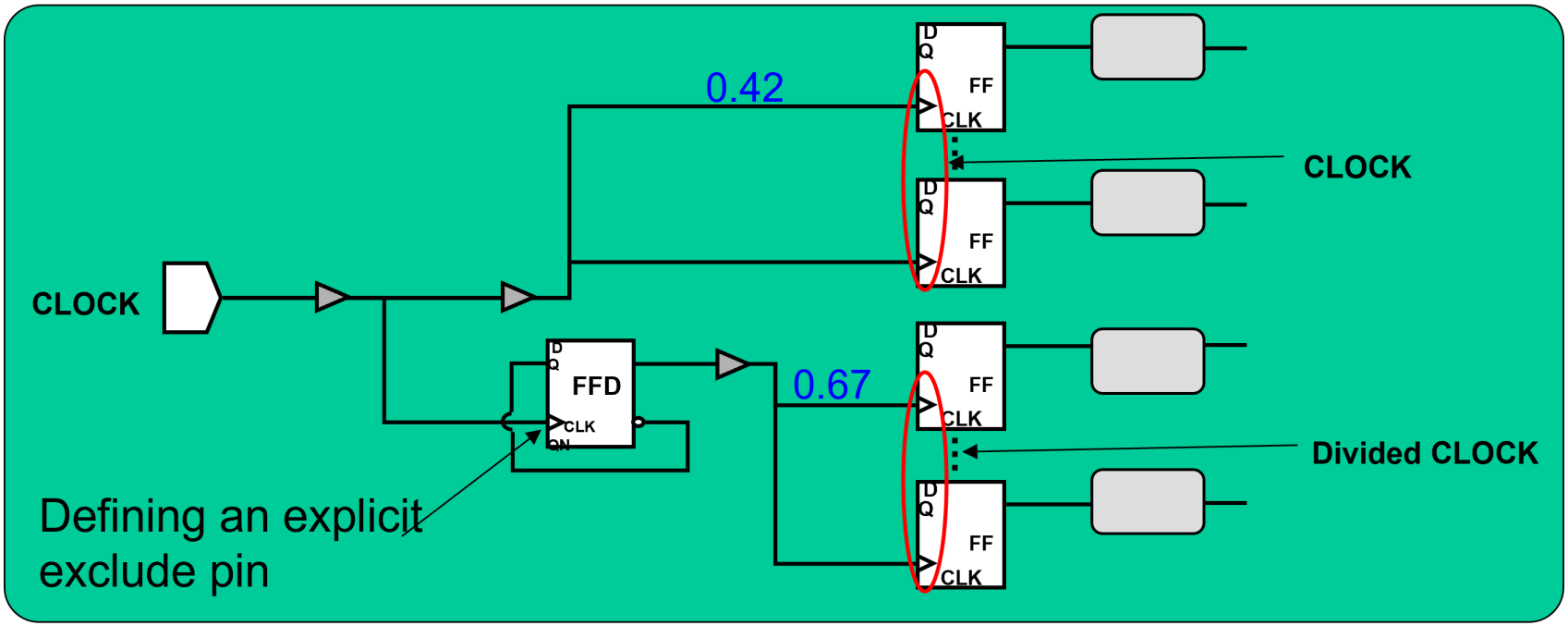
Generated and Gated Clocks



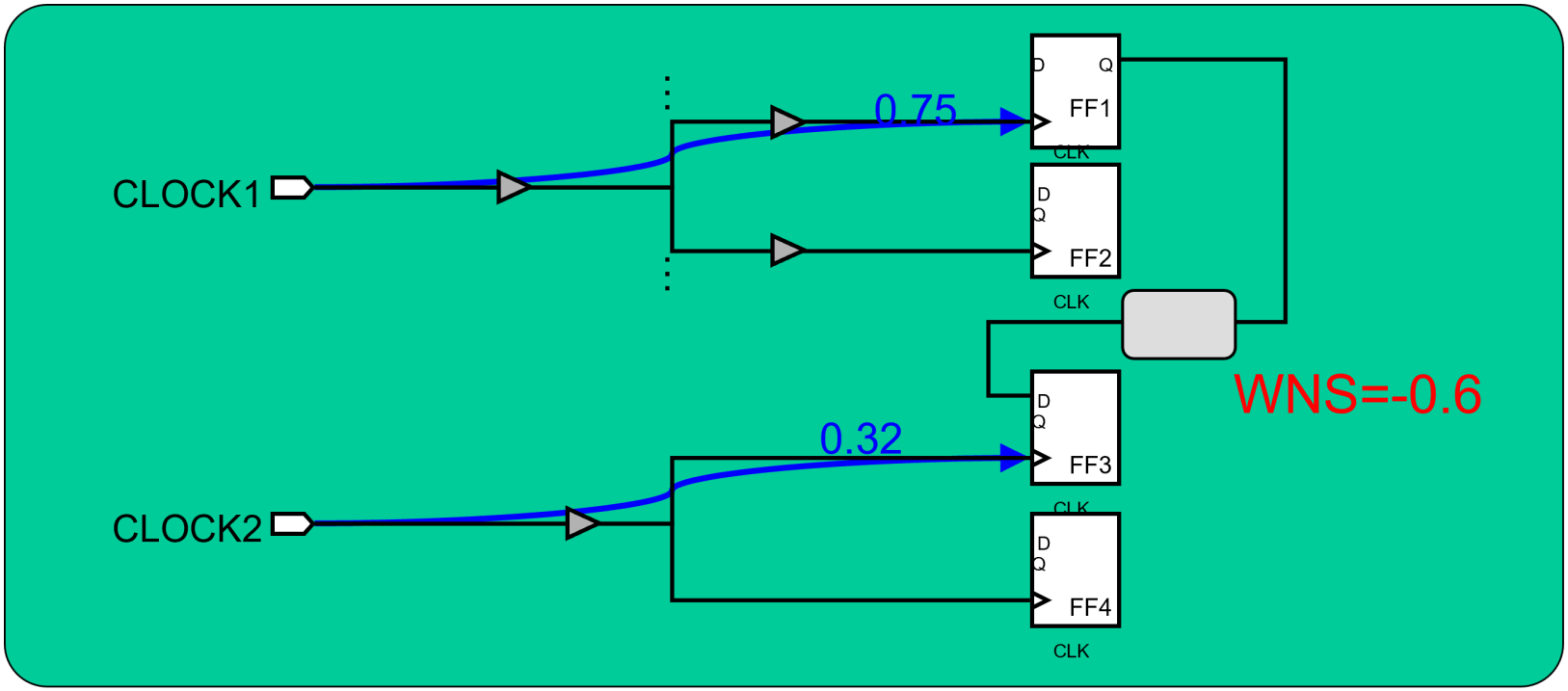
Skew will be balanced globally within each clock domain across all clock-pins for both master and generated clock.

Skew Balancing not Required

If the divided clock domain is independent of the master domain (no paths), then skew balancing may not be important.



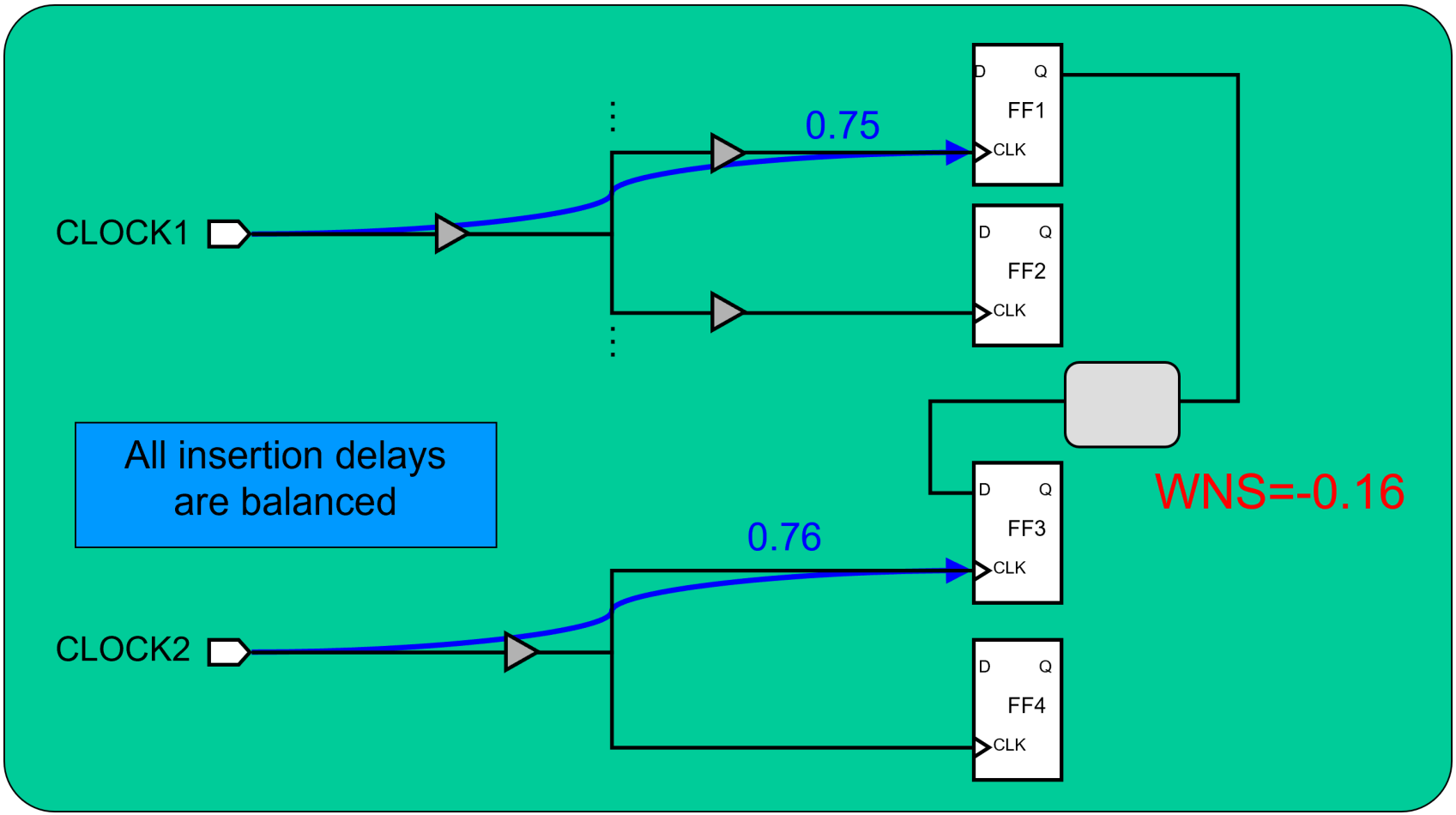
No Inter-Clock Skew Balancing by Default



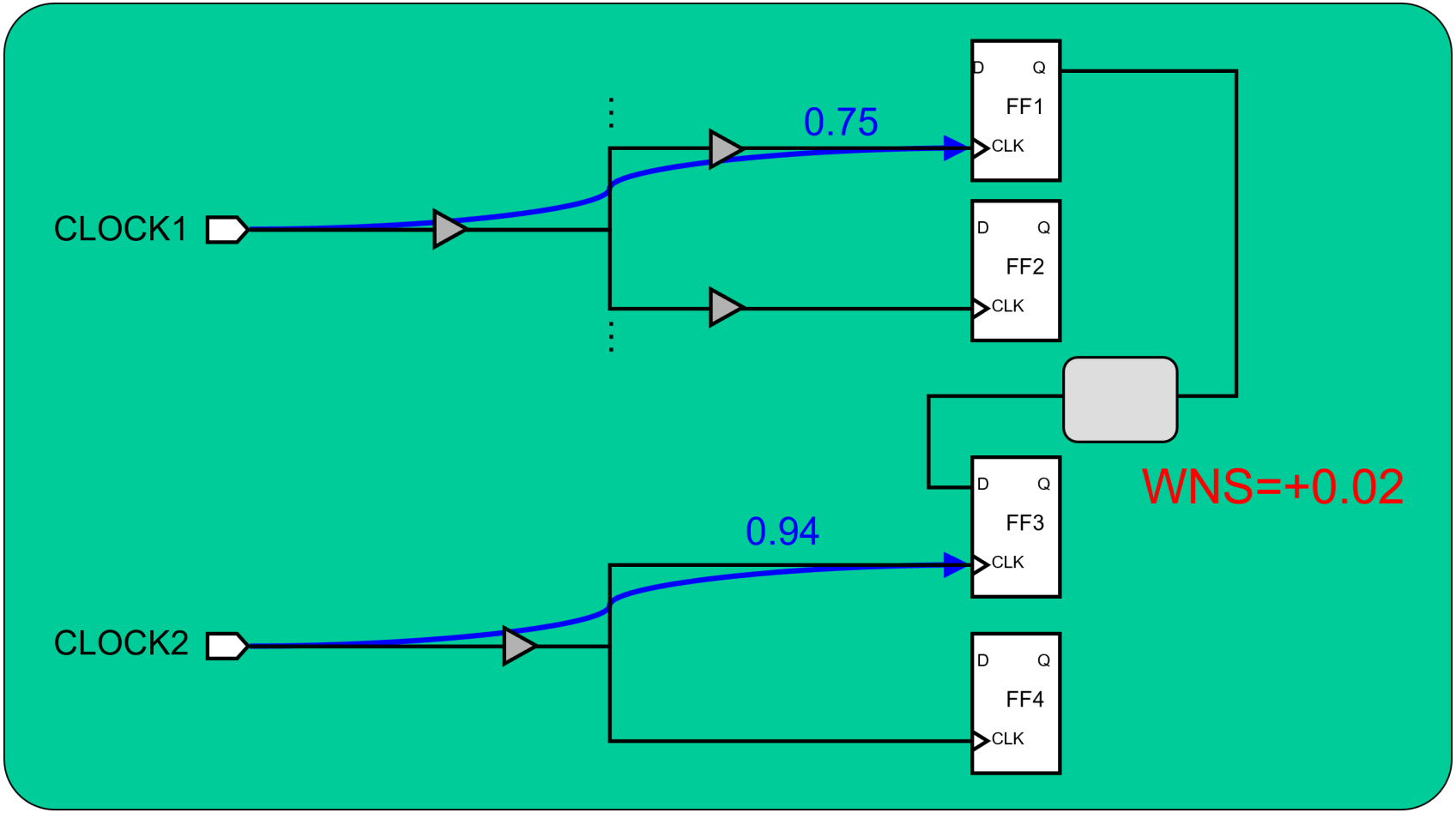
By default CTS does not perform inter-clock skew balancing → May result in worse setup timing violations

The path from FF1 to FF3 will have an additional setup penalty of 0.75-0.32=0.43

Inter-Clock Delay Balancing



Inter-Clock Delay Balancing: With Offset

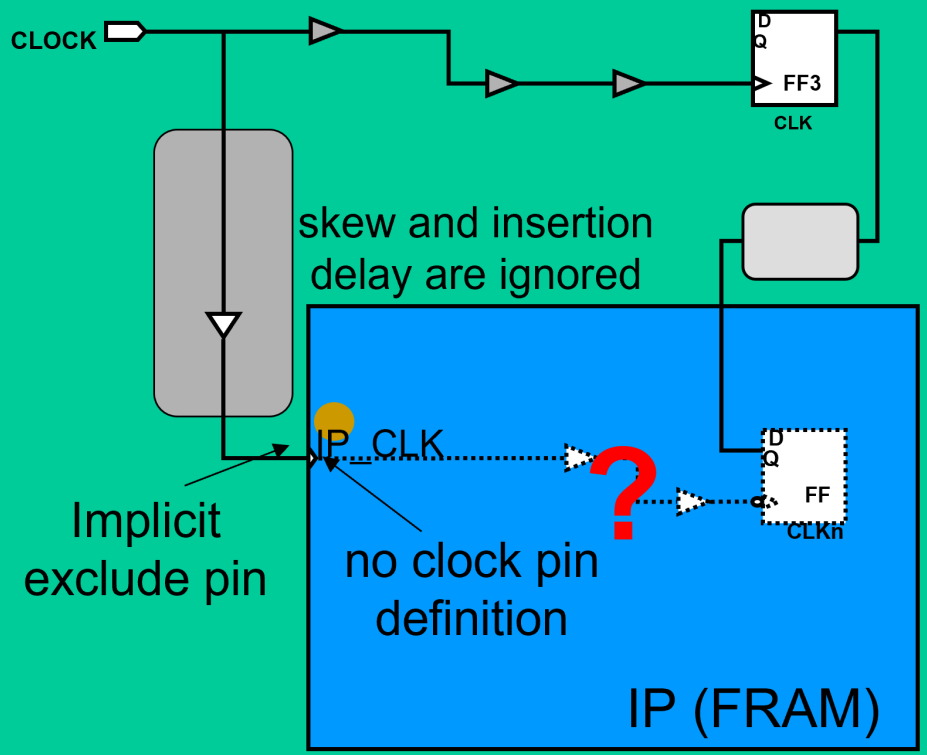


User-defined or Explicit Stop Pins

If the clock pin inside a macro cell is correctly defined, CTS will treat that pin as an implicit stop pin. In this example the clock pin is not defined.

What is the problem here?

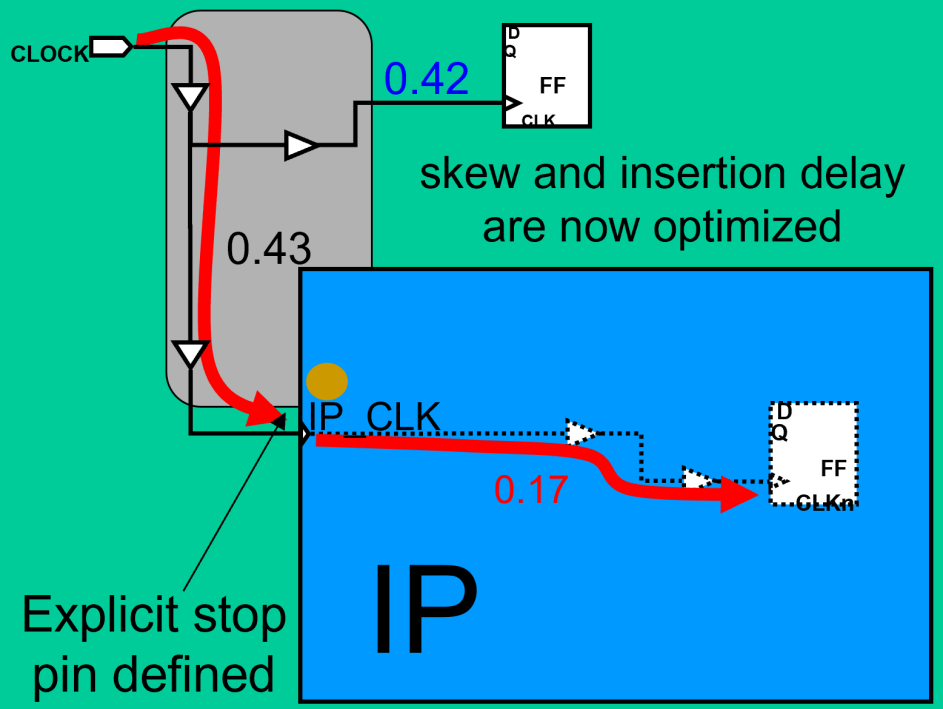
The macro's clock pin is marked as an implicit exclude pin – no skew optimization.



Defining an Explicit Stop Pin

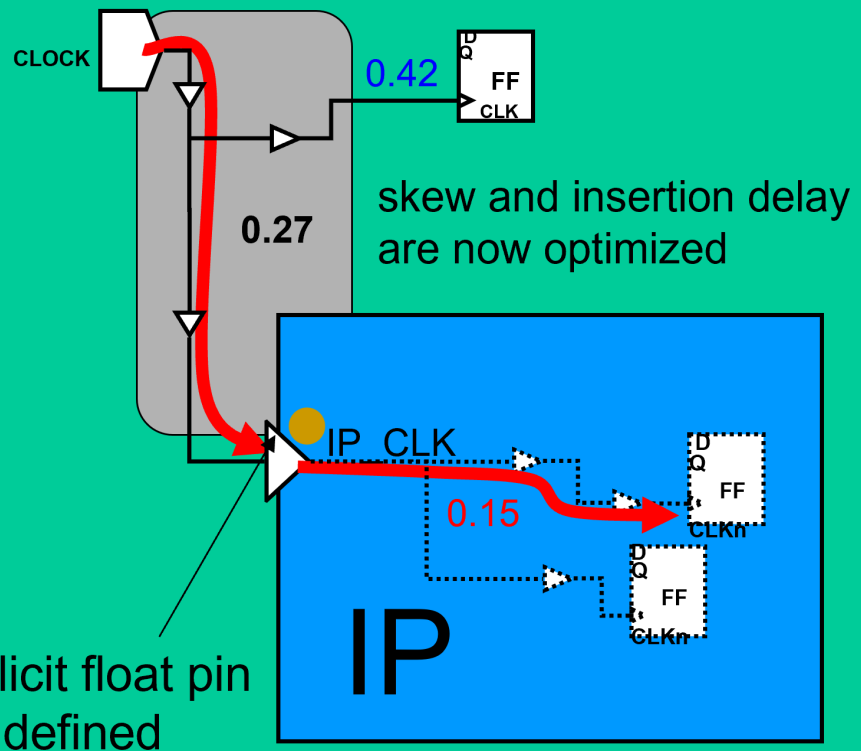
Defining an explicit stop pin allows CTS to optimize skew and insertion delay targets.

CTS has no knowledge of the IP-internal clock delay – it can only "see" up to the stop pin.



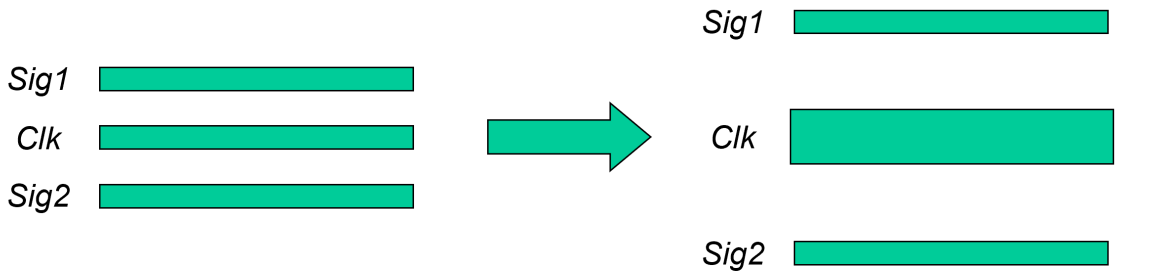
Defining an Explicit Float Pin

Defining an explicit float pin allows CTS to adjust the insertion delays based on specification.



Non-Default Clock Routing

- PnR Tool can route the clocks using non-default routing rules, e.g. double-spacing, double-width, shielding, and double via
- Non-default rules are often used to "harden" the clock, e.g. to make the clock routes less sensitive to Cross Talk or EM effects, which improve yield



Default Routing Rule ***Effect of NDR route on Clk***

NDR Recommendations

- **Always route clock on metal 3 and above**
- **Avoid NDR on Metal 1**
  - may have trouble accessing metal 1 pins on buffers and gates
- **Consider using double spacing to reduce crosstalk**
- **Consider double width to reduce resistance**
- **Consider double via to reduce resistance and improve yield**

Put NDR on Pitch for Accurate RC Estimation

- **Metal traces are always routed "on pitch"**
- **With clock NDR rules, pre-routing RC estimates of clock nets use NDR width and spacing numbers**
- **If NDR [spacing + width] numbers are not integer multiples of pitch (i.e. off-pitch), timing estimates pre-route may not correlate well with post-route timing**
- **Make sure your NDR numbers are on pitch!**

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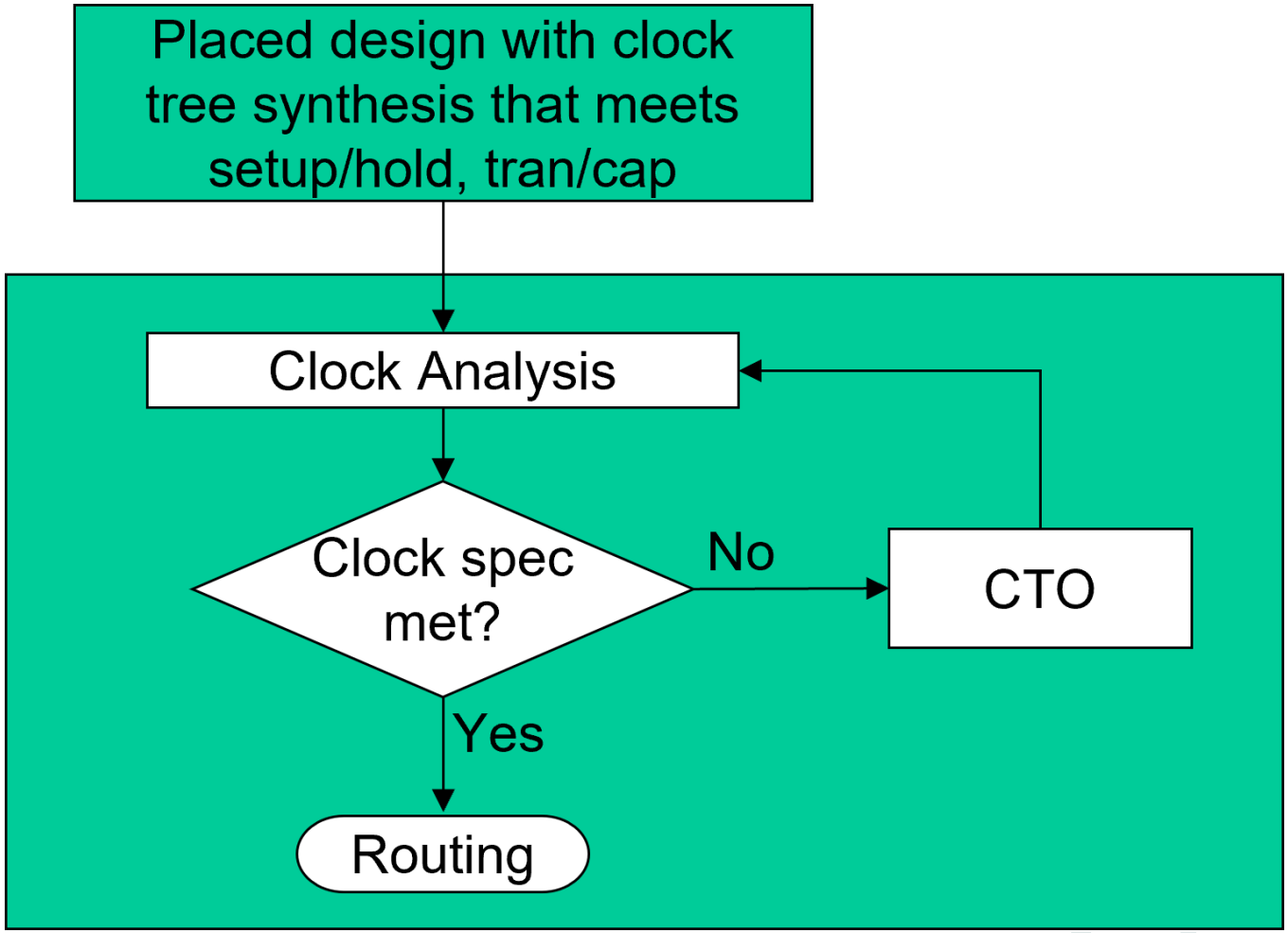
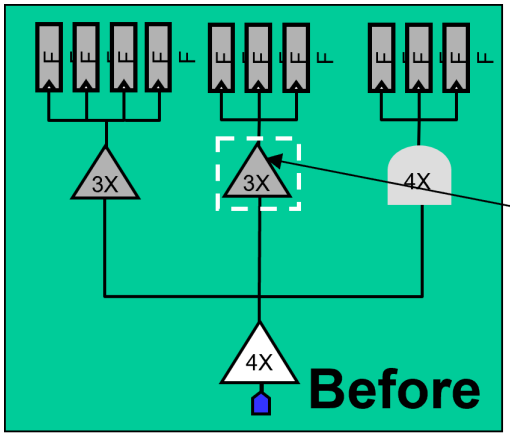
Clock Tree Optimization

Perform additional Clock Tree Optimization as necessary to further improve clock skew.



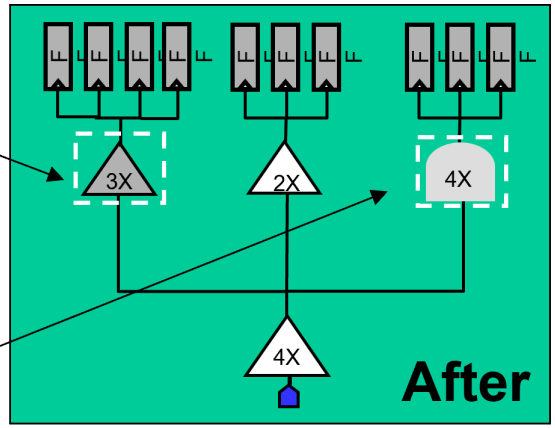
Clock Tree Optimization Options

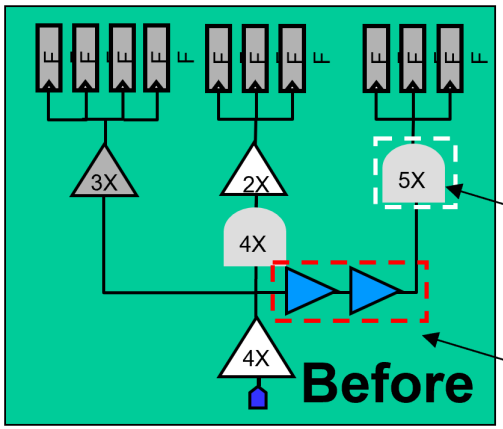


Buffer sizing

Buffer relocation

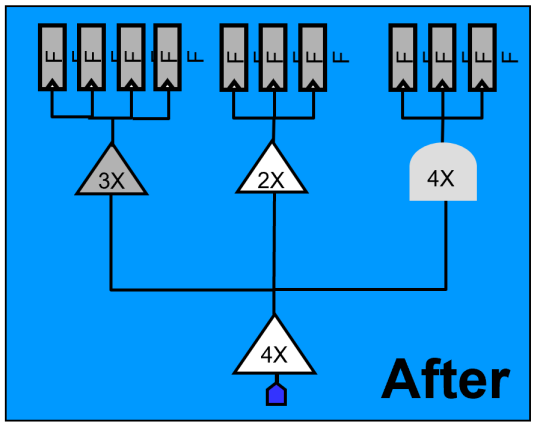
Gate relocation





Gate sizing

Delay insertion

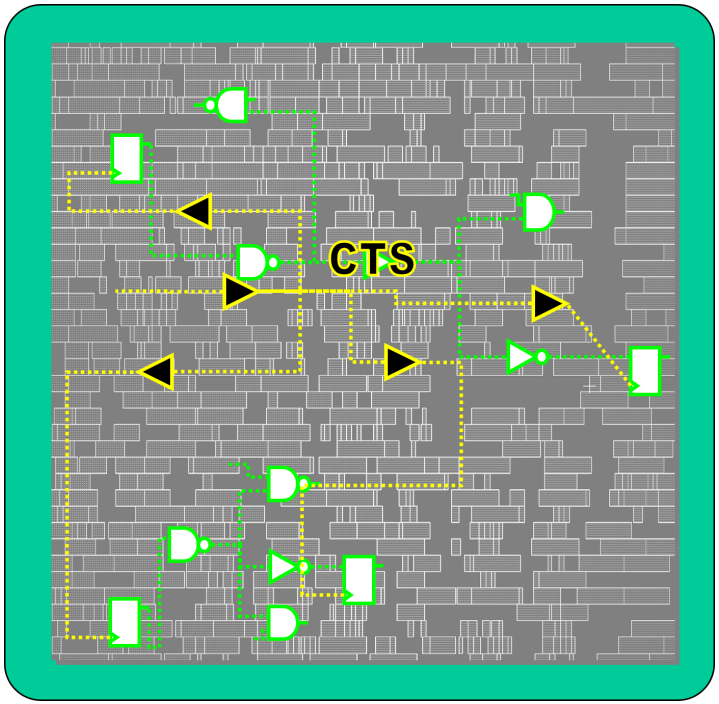


Analyzing CTS Results

- Report clock tree
  - Summary
  - Settings
  - ...
  - Reports max global skew, late/early insertion delay, number of levels in clock tree, number of clock tree references (buffers), clock DRC violations
- Report clock timing
  - Reports actual, relevant skew, latency, interclock latency etc. for paths that are related

Effects of Clock Tree Synthesis

- Clock buffers added
- Congestion may increase
- Non clock cells may have been moved to less ideal locations
- Inserting clock tress can introduce new timing and max tran/cap violations, which will be checked in the next stages



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بِسْمِ اللَّـهِ الرَحمَـن الرَحيمِ

وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا